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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/717,570	11/21/2000	Carol L. Thompson	10001151	2113

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
VU, TUAN A

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/717,570	THOMPSON, CAROL L.	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This action is responsive to the application filed November 21, 2000.

Claims 1-10 have been submitted for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hooker, USPN: 5,787,286 (hereinafter Hooker), in view of Blasciak, USPN: 5,265,254 (hereinafter Blasciak).

As per claim 1, Hooker discloses an apparatus to perform software performance checks opportunistically, the apparatus comprising:

first logic, such logic receiving a first set of instructions and generating an initial instruction schedule from such set, such first set including one or more instructions associated with a performance check function (e.g. col. 3, lines 21-25, lines 29-34 – Note: checking the pipeline for a empty placeholder or *bubble* to insert *tabulation* instructions is equivalent to scheduling logic operating on first set and including therein tabulation/performance instructions);

second logic, such logic evaluating the initial instruction schedule to determine whether the initial instruction schedule includes spare instruction slots into which said one or more instructions associated with the performance check function can be inserted (e.g. col. 2, lines 33-48; col. 3, lines 29-34); and

third logic inserting said one or more instructions associated with the performance check function into the spare instruction slots if enough spare instruction slots exist in the initial instruction schedule for accommodating said one or more instructions (e.g. col. 4, lines 12-37)

But Hooker does not specify that the performance checks or functions (*tabulation* instructions) thereof are correctness checking function. However, Hooker expresses the desirability for minimizing code insertion overhead or resources so as to not affect the performance of the code under analysis (e.g. col. 1, lines 34-56). Blasciak, in a system to insert instrumentation code to gather execution data and debug information using *dead areas* (e.g. *dead space*, Fig. 7; col. 9, lines 24-26) of code analogous to Hooker's use of *bubbles* to reduce overhead, discloses insertion of points at which to link instructions to measure execution statistics as well as instructions to verify correctness of time-based margins, references, context switches (e.g. col. 6, lines 30-37; col. 8, lines 30-36) and branch conditions (e.g. col. 8, lines 36-38). In view of the common intent by both Hooker and Blasciak, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement the code insertion technique as taught by Hooker such to add therein instrumentation code for correctness checking as suggested by Blasciak because a systematic and timely elimination of faulty references or memory inconsistencies, i.e. correctness checking, would further enhance the dynamic optimization of the code execution, improve performance and/or minimize additional resources usage or overhead for fault recovery which would otherwise be foiling performance evaluation as originally intended by Hooker.

As per claim 2, Hooker discloses a first logic generating initial code generation prior to initial instruction schedule, the correctness checking instructions being separated from other

instructions of such initial set of instructions (e.g. col. 1, line 63 to col. 2, line 11; col. 3, lines 16-25 – Note: executing the initial set of instructions with one distinct executing unit is equivalent to generating and scheduling the instructions into a pipeline of a RISC processor).

But Hooker does not disclose that the correctness checking function correspond to a conditional expression. But Blasciak's teachings from claim 1, e.g. the conditions checking for boundaries and branching (i.e. a conditional expression) for debug disclosing thereby the above limitation, would have render the above limitation obvious for the same corresponding rationale set forth in claim 1.

As per claim 3, Hooker (with Blasciak's teachings) discloses that said first, second and third logic correspond to executing a compiler program, such program including first code segment and generating the initial instruction schedule (col. 3, lines 21-34; step *11*- Fig. 1); a second segment for evaluating in said schedule to determine spare instructions slots existence; and a third segment for inserting correctness checking function instructions into the spare slots if enough such slots exist to accommodate such instructions (e.g. col. 2, lines 33-48; col. 3, lines 29-34; col. 4, lines 12-37; Fig. 1).

As per claim 4, this claim is the means claim version of claim 1 and includes the same limitations performed by the logics of claim 1 above; hence incorporates the corresponding rejections as set forth therein.

As per claim 5, this means claim corresponds to claim 2 above, hence is rejected herein using the same grounds as set forth therein.

As per claim 6, this claim is the method claim version of claim 1 and includes the same limitations performed by the logics of claim 1 above; hence incorporates the corresponding rejections as set forth therein.

As per claim 7, this method claim corresponds to claim 2 above, hence is rejected herein using the same grounds as set forth therein.

As per claim 8, this method claim corresponds to claim 3 above, hence is rejected herein using the corresponding rejections as set forth therein.

As per claim 9, this claim is the computer program claim version of claim 1, having computer-readable medium (also disclosed by Hooker: col. 6, lines 26-36) including code segments to perform the same limitations as in claim 1 above; hence incorporates the corresponding rejections as set forth therein.

As per claim 10, this computer product claim corresponds to claim 2 above, hence is rejected herein using the same grounds as set forth therein.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat No. 5,758,061 to Plum, disclosing boundaries checking code inserted at branching blocks.

U.S. Pat No. 5,551,001 to Cohen et al., disclosing snoop and consistency requests instructions at unused slots.

U.S. Pat No. 6,275,929 to Blum et al., disclosing filling unused delays insertion slots with useful instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703) 305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

or: (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
June 25, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100